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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/594,510	06/16/2000	Alan G. Wood	M4065.0184/P184	2407
24998	7590	01/25/2006	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			LUU, CHUONG A	
2101 L Street, NW			ART UNIT	
Washington, DC 20037			PAPER NUMBER	
			2818	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/594,510

Applicant(s)

WOOD ET AL.

Examiner

Chuong A. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-23,35 and 37-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23,35 and 37-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-23, 35 and 37-40 have been considered but are moot in view of the new ground(s) of rejection.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

### **The Rejections**

Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Yang (U.S. 6,498,387 B1).

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Yang discloses a wafer level package with  
(19) aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape;  
subsequently, connecting said semiconductor devices in said wafer to ball grid arrays on said dielectric tape;  
simultaneously dicing said wafer and said dielectric tape (see abstract. Figures 11-15);

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### **The Rejections**

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (U.S. 6,498,387 B1) in view of Gaynes et al. (U.S. 6,165,885).

Yang teaches everything above except for wherein said wafer is optically aligned with respect to said dielectric tape. However, Gaynes discloses an electronic component with (20) wherein said wafer is optically aligned with respect to said dielectric tape (see column 18, lines 51-65) It would have been obvious to one having

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ordinary skill in the art at the time the invention was made to modify the teaching of Yang (in accordance with the teaching of Gaynes) to optically aligned with respected to the dielectric layer during fabrication of a semiconductor device

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (U.S. 6,498,387 B1) in view of Smith (U.S. 6,300,149).

Yang teaches everything above except for wherein said wafer is magnetically aligned with respected to said dielectric tape; wherein oppositely charged magnetically elements are provided on said wafer and said tape; further comprising the step of locating a magnetic ring in a charged slot. However, Smith'149 discloses an integrated circuit with **(21)** wherein said wafer is magnetically aligned with respected to said dielectric tape (see column 4, lines 30-67); **(22)** wherein oppositely charged magnetically elements are provided on said wafer and said tape (see column 4, lines 30-67); **(23)** further comprising the step of locating a magnetic ring in a charged slot (see column 4, lines 30-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Yang (in accordance with the teaching of Smith's149) to magnetically aligned with respected to the dielectric layer during fabrication of a semiconductor device.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 103***

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### **The Rejections**

Claims 1-18, 35 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa et al. (U.S. 6,020,626) in view of Yang (U.S. 6,498,387 B1).

Ohsawa discloses a semiconductor device with

Respect to claims:

**(1); (11)** forming conductive structures (10b) in contact with a top surface of a dielectric substrate (8) (see Figure 10);

subsequently, forming a layered assembly by attaching a wafer (11b) to said dielectric substrate (8), such that said conductive traces (10b) are in electrical communication with semiconductor devices in said wafer (11b) (see Figure 10);

forming input/output devices (12b) in contact with said conductive traces (10b) (see Figure 10);

**(2)** further comprising the step of connecting said semiconductor devices to input/output devices (see Figure 10);

**(5)** wherein said step of forming said layered assembly includes the step of adhering said wafer to said dielectric substrate (see Figure 10);

**(6)** further comprising the step of electrically connecting said semiconductor

devices to ball grid arrays on said dielectric substrate (see Figure 10);

(7) wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric substrate (see Figure 10);

(8) wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said dielectric substrate (see Figure 10);

(10) further comprising the step of providing an electrode pad in said layered assembly (see Figure 10);

(12) wherein said forming step comprises the step of adhering said wafer to said metal layer (see Figure 10);

(13); (14) wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric substrate (see Figure 10);

(15) wherein said connecting step comprises the step of connecting solder bumps on said wafer to conductive traces on said dielectric substrate (see Figure 10);

(16) further comprising the step of connecting said traces to conductive vias extending through said dielectric substrate (see Figure 10).

(18) further comprising the step of testing said semiconductor devices through said ball grid arrays (see Figure 10);

(35) connecting said semiconductor devices to respective ball grid arrays located on said substrate (see Figure 10).

Horiuchi discloses everything above except for wherein said testing is conducted through said input/output devices and subsequently, dicing said layered assembly; adhering said wafer to a flexible substrate and further comprising the step of attaching

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said dielectric tape to said wafer by applying heat or pressure to the assembly.

However, Yang discloses a wafer level package with **(1)**; **(11)**.... subsequently, dicing said layered assembly (see abstract); **(3)** wherein said testing is conducted through said input/output devices (see abstract); **(4)** further comprising the step of discarding one or more defective packages; **(9)**; **(17)** wherein said dicing step is performed by a saw; **(11)**.... a stiff metal layer; **(35)** adhering said wafer to a flexible substrate; testing said semiconductor devices through said ball grid arrays (see column 4, lines 29-34); **(37)** further comprising the step of singulating packages from said wafer and said substrate (see column 4, lines 29-34); **(36)**; **(38)** further comprising the step of segregating defective packages from other packages (see column 4, lines 29-34); **(39)** further comprising the step of attaching said dielectric tape to said wafer by applying heat or pressure to the assembly (see column 4, lines 29-34); **(40)** further comprising the step of evacuating gas from said assembly. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Ohsawa (in accordance with the teaching of Yang) to attach the dielectric tape to said wafer by applying heat and pressure to the assembly; and further comprising the step of evacuating gas from said assembly during fabrication of a semiconductor device. Although, Ohsawa's reference is silent the step of testing semiconductor device; it would have been obvious that the testing should be taken place prior to further fabricating a semiconductor device. Doing so would facilitate the manufacture of the semiconductor device and reduce the time and cost by determining the defective device prior to complete the semiconductor device.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong Anh Luu  
Patent Examiner  
January 10, 2006